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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,061	02/11/2002	Donald C. Soltis JR.	10016639-1	6701

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,061	SOLTIS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 11-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *4-8 and 11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-8, 11-17 remain for examination. Claims 9.10 have been canceled.

2. Claims 4, 13, 15,16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. As to the newly amended claim 4, although claim 4 amended the data hazard detection circuit for detecting data hazards, no structural components of the data hazard detection circuit has been reflected into the claim, therefore, it is read as intended use and not the positive limitation of the claim. In addition, no substantial practical application for detecting the data hazards can be found in the claim.

4. As to the newly amended claim 7, claim 7 has shown a practical application by citing the identifying the data hazards reducing the dependency of the data hazards upon the size of the register file. Claim 7 is not rejected under "101" with a suggestion to change the clause "where" because "wherein" clause suggests optional and does not require the steps to be performed, and does not limit the scope of the claim .

5. As to claim 8, claim 8 is not rejected under "101" however, examiner would like to suggest amending the phrase such as "reducing the decency", or the like after the determination of the data hazards step to clarify the practical application of the method.

6. As to amended claim 13, although claim 13 recites the reducing of the dependency of a data hazards detection circuit within the processor , the practical

application of the evaluation of the mated entries is not clear. The examiner would like to suggest a positive limitation after the evaluating step.

7. As to newly amend claims 15, 16, similarly, the practical application of the determining the data hazards within the register file (claim 15) and the detecting data hazards (claim 16) is not clear. Therefore, claims 15,16 remain rejected under "101".

8. Claims 8, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fetterman et al. (5,627,985) in view of Kumar et al. (5,513,363).

9. As to newly amended claim 8, Fetterman also taught the register file and register ID file (see the (EAX) HEDN registers in fig.3 in the aliasing table) .

10. As to the newly amended claim 15, Fetterman also taught the register file and register ID file (see the (EAX) HEDN registers in fig.3 in the aliasing table) .

11. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (5,826,055) in view of Panwar (5,884,070) in view of Kumar et al. (5,51 3,363).

12. As to newly amended claim 4, the change is directed to clarify the language, and does not affect original scope of the claim.

13. Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadonato et al. (5,371,684) in view of Clift (6,598,149) in view of Lai (5,416,749) .

14. As to newly amended claim 7, Iadonato also reduced the dependency (see col.1, lines 39-68, col.2, lines 1-11).

15.

16. Claims 8,1 1,12, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar (5,884,070) in view of Kumar et al. (5,513,363) .

17. As to newly amended claim 8, see Panwar's fig.1B for the register fiel and register id file.

18. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Panwar (5,884,070).

19. The rejections are maintained and incorporated by reference the last Office action on 03/02/06.

20. The response filed on 06/02/06 has been fully considered but is not persuasive.

21. In the remarks, applicant argued that :

22. a) Panwar's f0 and f1 are consecutive;

23. b) Fetterman is one to one , not one to many aliasing;

24. c) no comparison of register id to determine the data hazards in Fetterman, the valid bit is not register id;

25. e) Fetterman did not teach data hazards;

26. f) Wang is directed to detection of instruction dependencies , not data hazards I bypass data;

27. g) Kumar did not teach he aliasing of two or more non-consecutive registers ;

28. h) Wang's tag did not correspond to registers ;

29. i) Iadonato did not teach register file ID, and the addresses were not aliased;

30. j) consecutive rows were accessed simultaneously in Lai, no row –to-row for two or more non-consecutive rows was possible;

31. k) Lai was a sequential access which would not be appropriate for Iadonato;

32. l) Panwar would increase the size of detection circuit.

33.

34. As to a) above, the definition of "consecutive" is not clearly set in the claim. As to a) above, Panwar's f0 and f1 are non-consecutive because it were separately designated as two separate single precisions registers. The starting bit of register f0 , bit 0, and the starting bit of register f1 , bit 32, are not consecutive.

35. As to b), Fetterman taught his EAX register mapping to corresponding physical register and real register in a single entry of EAX (see col.8, lines 41-49) . Therefore, each register was one to many registers (physical register and virtual register).

36. As to c), Fetterman taught his valid bit was used to indicate whether the corresponding bit was retired to the appropriate committed state register (se col.8, lines 45-49). The valid bit must be an identifier or part of the identifier , for the corresponding register for purpose of determining the retire condition of the register.

37. As to e), Fetterman taught the committed state registers stored the speculative execution results (see col.3, lines 29-35). Therefore, it indicated data hazards.

38. As to f), Wang taught a dependency checking for checking the instruction dependencies to be executed (see col.6, lines 57-67) . The dependencies were data hazards. The bypass data was already taught by Wang in col.10, lines 1-5).

39. As to g), Kumar was used to supplement the teaching of the non-overlapping size of the register groups (see col.3, lines 1-13, col.7, lines 31-41). The reasons of obviousness were already given in paragraph 21 of the last office action on 03/02/06, therefore, it will not be repeated herein.

40. As to h), Wang taught a register ID file (see the TAG generated by RRC 204 in col.9, lines 9- 46, see the RRC 204 for facilitating the hazard detection in col.7, lines 5-24). Therefore, The tag did correspond to registers.

41. As to i), Iadonato taught compared the addresses of the registers for providing hazard detections (see fig.2 108) by common detection logic (see how the conflict of the source and destination registers being detected in col.6, lines 63 col.7, lines 1-20) . Therefore, It was a register ID file. No aliasing has been claimed in claim 7.

42. As to j), Lai taught tags used to identify those registers which contained floating point (see col.3, lines 40-49). Therefore, row–to-row for two or more non-consecutive rows was possible, such as the all odd rows.

43. As to k), Lai taught simultaneous access of two or ore rows (see col.2, lines 62-68, col.3, lines 1-2). Therefore, Lai was appropriate for Iadonato.

44. As to l), Panwar taught the number of dependencies per instruction was reduced , thereby reducing the processor resources (see col.10, lines 28-37). Therefore, the detection circuit size must be reduced.

45. Claim 1 is allowable over the art of record for reciting the combined detailed features of the identifying the first group of registers , aliasing the first group of registers, the detection of the data hazards associated with the group of identifiers, the aliasing of the second group of registers to the group of identifiers, the detection of the data hazards associated with the group of identifiers within the data hazard detection circuit. The preamble reciting the aliasing of the stack of registers of a register file of a processor within the data hazard detection circuit of the processor to reduce the dependency of the data hazard detection circuit upon size of the register file shows the practical application of the method, therefore has overcome the "101" rejection with a suggestion to the applicant also recite the reducing of the dependency in the body of the claim to clarify positive limitation of the claim.

46. Claims 13-14 are allowable, upon pending condition of the "101" above, over the art of record for ' selecting register file id size, aliasing at least one entry of the register ID file to two or more registers of the register file, each of the two or more registers being located in a non- overlapping group of sequential registers equivalent in size to the over selected resister ID file size; and evaluating matches between entries of the register ID file in the hazard circuit without distinguishing between common aliased entries of the register file.

47. Claim 16 is allowable, upon pending condition of the "101" above, over the art or record for reciting a method of stack register aliasing in data hazard detection Circuit in a processor, comprising aliasing two or more non-overlap groups of consecutive registers of a stacked register file to one group of consecutive register IDs within the data hazard detection Circuit each register ID aliasing one register from each group of consecutive resisters', and detecting data hazards, if any, associated with y first and second register of the stacked register file by comparing a first aliased register ID of the first register to a second aliased register ID of the second register within the data hazard detection circuit.

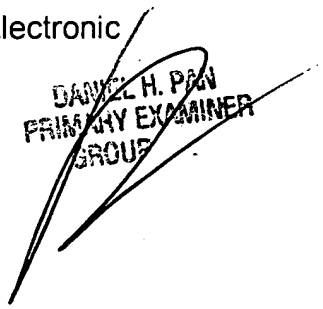
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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